AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0014] with the following new paragraph [0014].

[0014] FIG. 1 is a block diagram illustrating a structure of a semiconductor device with a speed binning test circuit that performs a speed-binning test, according to an exemplary embodiment of the present invention. Referring to FIG. 1, the semiconductor device, which in FIG. 1 is embodied as a chip, for example, may include a plurality of signal input/output (I/O) pins 101-108, which are the same as those installed in a general semiconductor device, for example. Signals may be input to the signal I/O pins 101-108 from a core circuit 110, and/or signals may be output from the signal I/O pins 101- 108 to the core circuit 110. The core circuit 110 performs given functions using its logic circuit and receives/outputs signals from/to the plurality of signal I/O pins 101- 108.

<remainder of page intentionally left blank>